

# A novel controller for switching audio power amplifier with digital input

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*Abstract- A new controller, Bi-directional Saw-tooth Error Correction (BSEC) for switching audio power amplifier with digital PWM input is proposed. This control method is based on a pulsed edge correction approach using PWM audio signal input as a reference for power switching digital to analog converter. The proposed controller has excellent features such as wide error correction range and no limitation on the modulation index. The controller is implemented in the half-bridge class D amplifier and the performance is verified through hardware experiments. It delivers 100W into 4Ω load with less than 0.2% of total harmonic distortion (THD) all over operating range with the maximum efficiency of 82%.*

## I. INTRODUCTION

Digital storage of audio signals has enabled high quality recordings to be made available to the public; for example, compact discs, digital audiotapes, DAT and DCC, and digital broadcasts, near instantaneously companded audio multiplex (NICAM), all use digital form signal processing. However, conventional reproduction of the sound requires conversion from digital to analog (D/A), followed by analog amplification. These have limited opportunities for improvement, and are costly to implement for low noise or for high dynamic range [1]. Recently, there have been some trials to achieve power amplification without signal D/A converter (DAC). For the solution, many researches [1-4] have proposed to implement PCM(Pulse Code Modulation)/PWM conversion of digital audio source, followed by direct PWM power amplification such as class-D type switching amplifier.

This approach uses PWM signals of PCM/PWM converter as the reference for the power amplifier instead of analog signals. Thus, these researches have been focusing on the performance progress of PCM/PWM converters to obtain clear reference of power stage. This method gives some merits such as simple structure, and cost reduction because the digital signal processor directly giving PWM signal replaces DAC and PWM-generating carrier modulator utilized in conventional switching amplifier processing. As this approach allows simplifying output stage feedback

processing for error compensation, it helps to integrate the whole structure of the amplifier.

Following the digital signal processing part, usually class-D type switching amplifier is used in order to convert the digital PWM source directly into audio power because of the power efficiency profit [5]. However, even though the digital modulator performance shows excellent linearity, power amplifier stage cannot reproduce the level of linearity without feedback correction network because there are many potential distortion sources. Therefore, recently, some researches to advance the linearity performance of class-D audio power amplifier have been published [3,6,7].

## II. Conventional power stage error correction

In spite of clear PWM reference, pulse distortions diminishing the fidelity of audio output are introduced in the switching power stage by some kinds of nonlinear disturbances. In fact, practically realized class-D type open-loop power amplifiers have generally about 0.1% - 2% THD level. This THD level originates from error sources in power stage, which are categorized such as pulse timing error (turn-on and turn-off delay, dead time, finite rise and fall times) and pulse amplitude error (power supply perturbations, finite power switch impedance)[3]. Therefore, it is necessary to correct errors efficiently by negative feedback loop.

Simply thinking, direct feedback to the digital PCM reference seems reasonable for audio sound to chase the

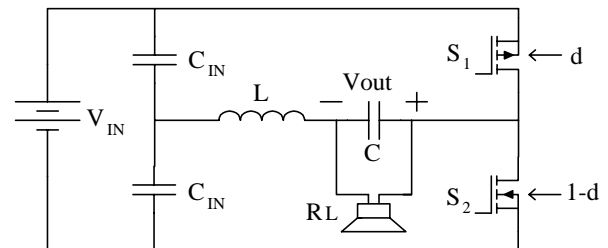


Fig. 1 Power stage configuration

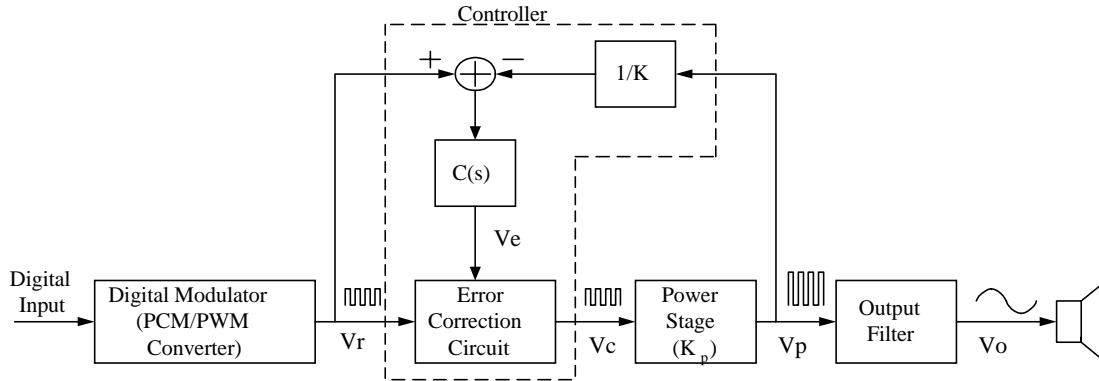


Fig. 2 Controller block diagram

original digital audio source. However, this approach requires A/D converter in feedback path to convert analog audio output to digital signal format to be compared with the PCM reference [3]. Since A/D converter restricts cost and performance competences in the same manner as D/A converter, the feedback into PWM signal - the DSP output point - is more attractive than the direct digital feedback, providing that the DSP offers pulsed reference with negligibly distorted information.

Nielsen has proposed Pulse Edge Delay Error Correction (PEDEC) controller to correct power stage errors using PWM reference given by PCM/PWM modulator [3]. Simulation model of this configuration shows successful elimination of high quality D/A converter and external triangular generator. However, this method has some limitations, such as restricted error correction range and limited duty ratio. Hence, it cannot properly operate at the wide input voltage variation and large amount of perturbation. Furthermore, PEDEC controller requires fast transition of modulation waveform ( $V_m$  of fig. 3(b)), which restricts realizable maximum switching frequency in a practical viewpoint.

In this paper, a new pulse referenced control method, which is named Bi-directional Saw-tooth Error Correction (BSEC) and suitable for digital pulse modulation based power amplification is suggested. This method has the following advantages: wide error correction range, high gain of error correction circuit, possible high switching frequency and no limitations in minimum/maximum duty ratio.

### III. PRINCIPLE OF THE PROPOSED CONTROLLER

The power stage considered in this work is the half-bridge class-D amplifier, shown in fig.1. The output voltage,  $V_{out}$  :

$$V_{out} = \frac{V_{IN}}{2} \cdot d - \frac{V_{IN}}{2} \cdot (1-d) = V_{IN} \cdot \left( d - \frac{1}{2} \right) \quad (1)$$

where  $d$  is the duty ratio of the upper power switch  $S_1$  and  $1-d$  is that of the lower switch  $S_2$ . If the duty ratio is

modulated with audio signal and the switching frequency is much higher than audio band frequency, the switching ripple is removed by the output LC filter, and only the average value of pulse waveform is delivered to speaker. Thus, the output voltage can follow the audio source information. If pulse errors caused by the power stage is properly corrected, the natural linearity of this power stage can be better than that of a typical class AB amplifier in which the distortion has the range of 0.1% ~ 2%[3]. This class-D type half-bridge inverter operates in synchronous rectification mode to maintain high efficiency usually above 80% at full load.

As the feedback error control method of this power stage, the new error correction scheme, BSEC is introduced. Its block diagram and operating principle are shown in fig. 2, fig. 3, respectively. The PCM/PWM converter with high quality audio information generates the PWM signal,  $V_r$  in fig. 2. BSEC unit uses it as a reference for error correction. For the negative feedback control, power stage output  $V_p$  is sensed and attenuated by the sensing gain  $1/K$  and, compared with the reference  $V_r$ . The compensator block,  $C(s)$  in fig. 2, offers the error information  $V_e$  that results from the pulse timing error and pulse amplitude error of  $V_p$ . The error correction circuit unit receiving  $V_e$  and  $V_r$  produces the error corrected pulse signal,  $V_c$ , which drives the power switches  $S_1, S_2$ . Table 1. arranges every major parameters in fig 2.and fig. 3 with their descriptions.

Table 1. Definitions of BSEC parameters

Parameter	Description
$V_e$	Control error signal to BSEC unit
$V_r$	Digital modulator output as reference signal
$V_c$	BSEC unit output voltage
$V_p$	Power-amplified pulse signal
$V_m$	Bi-directional saw-tooth waveform for error correction
$k_a$	Slope of $V_m$
$T$	Switching period
$D$	Duty cycle of $V_c$
$V_{IN}$	Power rail voltage
$T_w$	Pulse width of $V_r$
$T_a$	Pulse width of $V_c$

For the description of the principle of proposed controller, fig. 3 illustrates major waveforms of the error compensation block. BSEC error compensation is achieved by pulse edge re-timing approach that is the similar concept of PEDEC [3]. As the average value of the output voltage depends on the pulse width of  $V_c$ , it is possible to compensate for the output stage error by controlling the pulse edge timing of  $V_c$ . The principle of BSEC is well illustrated in the waveforms of fig. 3(a).

To change duty from the reference by error information, a slope waveform is needed such as saw-tooth shaped modulation signal ( $V_m$ ) of BSEC. To achieve the shaping of modulation signal, simply the reference pulse signal is utilized as a parent signal. The negative saw-tooth part of  $V_m$  is formed with a constant slope  $-k_a$  during the positive reference signal. When the reference changes the polarity, BSEC makes  $V_m$  zero instantly. While  $V_r$  is negative, BSEC generates the positive saw-tooth of  $V_m$  with the slope  $k_a$ . The BSEC unit generates the error-corrected PWM signal ( $V_c$ ) by comparing error signal ( $V_e$ ) with the modulation signal. Driven by this signal ( $V_c$ ), the power stage can derive high-fidelity reproduction of audio signal ( $V_o$ ) through low-pass filtering of the amplified pulse waveform ( $V_p$ ). In this manner, the  $V_p$  sensing feedback network compensates all distortions in the amplifier except the error occurring in the output post LC filter.

PEDEC [3] is also shown in fig. 3(b). In the case of PEDEC, there are some restrictions that the minimum pulse width ( $T_w$ ) should be wider than the transition time of  $V_m$  ( $T_o$ ). And, the corrected pulse width ( $T_b - T_w$ ) cannot exceed the transition time. These result in a limited error correction range within the transition time and restriction on the

minimum/maximum duty ratio. The modulation index ( $M$ ) is limited such as eq. (2) [3]:

$$M_{\max} = 1 - \frac{2T_o}{T} \quad (2)$$

And the PEDEC controller function FM is:

$$FM = \frac{\Delta V_{C,AVE}}{\Delta V_e} = \frac{2 \cdot T_o}{V_M \cdot T} \quad (3)$$

where  $V_M$  is the amplitude of  $V_m$ ,  $V_{C,AVE}$  is the average of  $V_c$  when the amplitude of  $V_c$  is 1. As shown in eq. (2) and eq. (3), transient time span ( $T_o$ ) gives a trade-off between modulation index and controller gain at a given switching period and a given  $V_M$ . Therefore, wide modulation factor gives a restriction that prevents the controller gain from high value.

Another inevitable limitation is the offset delay with no correction of  $T_o/2$  [3]. This property reduces error response speed, and makes output delay from sound source. It can give a negative effect on the feedback performance. This is because the  $V_c$  delay induces the delay of  $V_p$ , the phase difference between  $V_p$  and  $V_r$  makes switching frequency ripple on  $V_e$  different from DC assumption. In extreme case, the ripple makes  $V_e$  exceed the magnitude of  $V_m$ , and the error control is not effective as expected. Thus, the smaller delay is desirable for the feedback performance.

In the case of the proposed Bi-directional Saw-tooth Error Correction(BSEC), the effective change in pulse width:

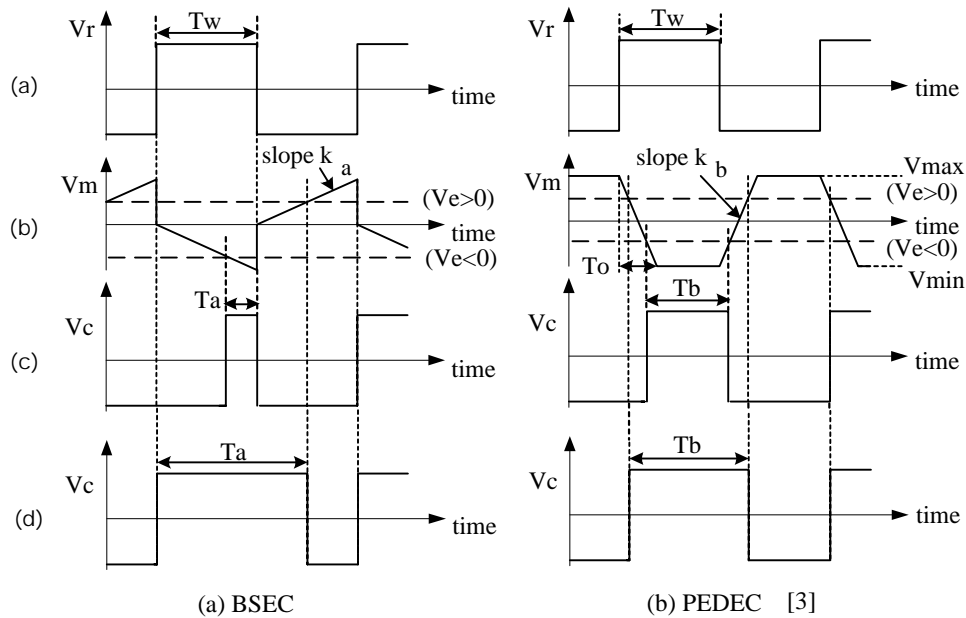


Fig. 3 Error correction schematics of BSEC and PEDEC  
 ((a): reference pulse, (b): modulation waveform, (c): output pulse when  $V_e > 0$ , (d): output pulse when  $V_e < 0$ )

$$\Delta T_w = T_a - T_w = \begin{cases} (1-D) \cdot T & (V_e > k_a(1-D)T) \\ \frac{V_e}{k_a} & (-k_a DT \leq V_e \leq k_a(1-D)T) \\ -DT & (V_e < -k_a DT) \end{cases} \quad (4)$$

where  $T_a$  is the corrected pulse width and  $k_a$  is the slope of  $V_m$ . Hence, the following relationship between  $T_w$  and  $V_e$  is established:

$$\frac{\Delta T_w}{\Delta V_e} = \frac{1}{k_a} \quad (5)$$

This equation shows that the effective change in pulse width ( $\Delta T_w$ ) is proportional to the error voltage ( $V_e$ ). Therefore, FM is expressed as the slope  $k_a$  and the switching period ( $T$ ) as follows:

$$FM = \frac{\Delta V_{C,AVE}}{\Delta V_e} = \frac{2}{k_a \cdot T} \quad (6)$$

And, the resulting form of the closed loop gain of the proposed controller is:

$$G_{cl}(s) = \frac{K_p}{K} \cdot C(s) \cdot FM \quad (7)$$

where  $K_p$  is the power stage gain when the amplitude of  $V_c$  equals 1,  $1/K$  is the feedback sensing gain,  $C(s)$  is the compensator transfer function. This scheme eliminates the limitations of PEDEC mentioned above. There are no limitations on the minimum/maximum duty ratio and error correction range in the BSEC operation. It means this scheme allows designing wide input range system with BSEC. In addition, there is no requirement to compromise between the modulation index and the controller gain, thus high modulation index design is possible with high gain controller. According to this condition, the total closed loop gain of the BSEC can be designed larger than that of the PEDEC, and eventually this condition improves the fidelity of audio sound by increased closed loop gain suppressing the sensitivity of harmonic distortion. In practical realization viewpoint, BSEC is profitable for high frequency switching schematics. At the same operating point (same reference duty and same controller gain), saw-tooth of BSEC controller has half the tangential slope compared with PEDEC case because the modulation slope runs from positive amplitude to negative in PEDEC case while bi-directional saw-tooth slope runs from zero point. This means that the twice switching frequency is possible when the same tangential slope is realized in case of BSEC.

About delay characteristic of BSEC, there is no time delay with no correction case. And, BSEC has a tendency that as error correction degree rises, delay time increases as well.

Considering the feedback loop shaping, this has a trade-off

between stability and system performance such as loop gain and loop bandwidth. Since audio system requires the audio bandwidth over about 20kHz, the crossover frequency of the loop should be higher than audio bandwidth. In addition, the closed loop gain should be as high as possible around the bandwidth. Also, the phase margin is desired at least 45 degree to guarantee the system stability. Another constraint is that the frequency range higher than crossover point should have low gain as much as possible to diminish high frequency noise in the loop. In this case,  $C(s)$  is a high DC-gain two-pole configuration for circuit simplicity and good ripple rejection. Excessive poles can make system unstable. The resulting closed loop transfer function is as follows:

$$G_{cl}(s) = \frac{K_p}{K \cdot T \cdot k_a} \cdot \frac{K_c}{\left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p2}}\right)} \quad (8)$$

For a high loop gain,  $K_c$  must be a high value for the enhancement of the error correction capability. Note that the switching period also influences on the control system, inversely proportional to the loop gain. Since the peak value of general open loop THD is  $-30\text{dB}$  or  $-40\text{dB}$  level, the minimum closed loop gain for the audio-band frequency should be at least  $30\text{dB}$  for closed loop THD to reach  $-60\text{dB}$  level required by high fidelity application.

#### IV. THE PRACTICAL REALIZATION AND PARAMETER DESIGN OF BSEC UNIT

The circuit realization of BSEC unit is illustrated in fig. 4. BSEC unit is composed of a comparator and a pair of generators that make positive and negative saw-tooth, and a differential amplifier.

The circuit operation has only 2 modes that make positive

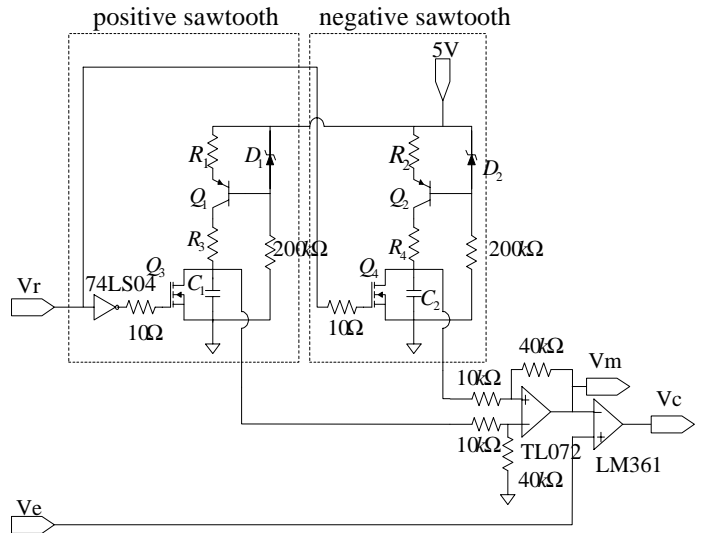


Fig. 4 Implemented BSEC circuit

and negative saw-tooth in each mode: In high level Vr mode, as Q<sub>3</sub> turns off and Q<sub>4</sub> turns on, the constant current source composed of Q<sub>1</sub>, R<sub>1</sub>, R<sub>3</sub> charges C<sub>1</sub> while C<sub>2</sub> discharges and maintains zero voltage through Q<sub>4</sub>. Voltage of C<sub>1</sub> increases linearly and the output of the differential amplifier decreases linearly. The moment Vr turns to the low level, Q<sub>3</sub> turns on, and discharges C<sub>1</sub> instantly. Then, the output of differential amplifier Vm rises into zero simultaneously and a negative saw-tooth waveform is obtained.

Low-level Vr mode operation is dual with the high-level mode: C<sub>2</sub> voltage increases linearly and C<sub>1</sub> keeps zero voltage, and the differential amplifier voltage increases linearly. The moment Vr turns to the high level, Vm falls into zero instantly and positive saw-tooth is derived. These operations are repeated cycle-by-cycle to generate the bi-directional saw-tooth waveform continuously. The intended slope of the saw-tooth determines parameter values of the constant current source and values of the charging capacitors as well as the gain of the differential amplifier. Therefore, to design high gain of BSEC unit, the slope k<sub>a</sub> should be small by a large C<sub>1</sub> (C<sub>2</sub>) value and low current level of source. Or a small gain of the differential amplifier is also a good choice for high controller gain. However, large C<sub>1</sub> (C<sub>2</sub>) makes considerable discharging time and loss. Moreover, excessively low slope weakens the immunity of the ramp (Vm) to the ripple of error voltage (Ve). Effects of ripple become pronounced as ripple amplitude approach to the saw-tooth amplitude.

Table 2. Major design parameter values

Components	Parameters	Components	Parameters
R <sub>1</sub> , R <sub>2</sub>	200Ω	R <sub>3</sub> , R <sub>4</sub>	500Ω
Q <sub>1</sub> , Q <sub>2</sub>	2N2907	Q <sub>3</sub> , Q <sub>4</sub>	2N7000
D <sub>1</sub> , D <sub>2</sub>	1N5225	C <sub>1</sub> , C <sub>2</sub>	4nF
$f_{p1} = \omega_{p1} / 2\pi$	7.4kHz	$f_{p2} = \omega_{p2} / 2\pi$	37kHz
K <sub>p</sub>	40	K	25

## V. EXPERIMENTAL RESULTS

A 100W switching audio power amplifier with digital input was implemented using the new controller. The power stage parameters are as follows: V<sub>IN</sub>=80V, C<sub>IN</sub>=4700uF, L=10uH, C=0.1uF, S<sub>1</sub>=IRF9530, S<sub>2</sub>=IRF530, 4Ω load, 360kHz switching frequency. The compensator C(s) has dc gain of 100 and overall closed loop dc gain is 25 with two poles at 7.4kHz and 37kHz. The power stage gain (K<sub>p</sub>) and the feedback sensing gain (1/K) are 40 and 1/25, respectively. A design example of major parameter values of the controller is shown in table 2.

The measured THD curves are plotted in fig. 5 for the full audio frequency range from 20Hz to 22kHz and for various output power by using an audio precision equipment. The THDs of the amplifier are all below 0.2%, and the highest THD occurs at full power, 7kHz. When the power supply

voltage for the amplifier is half the nominal value, the amplifier shows almost the same THD (not shown) as fig. 5 up to 20W level by virtue of the wide correction range of the new controller. Figure 6 shows the measured amplifier power stage efficiency using the audio precision tester to calculate output power into a resistive 4Ω load. The efficiency of the amplifier was 82% at full power and 79% at half power. This high efficiency contributes to considerable hardware size reduction by removing bulky heat sink.

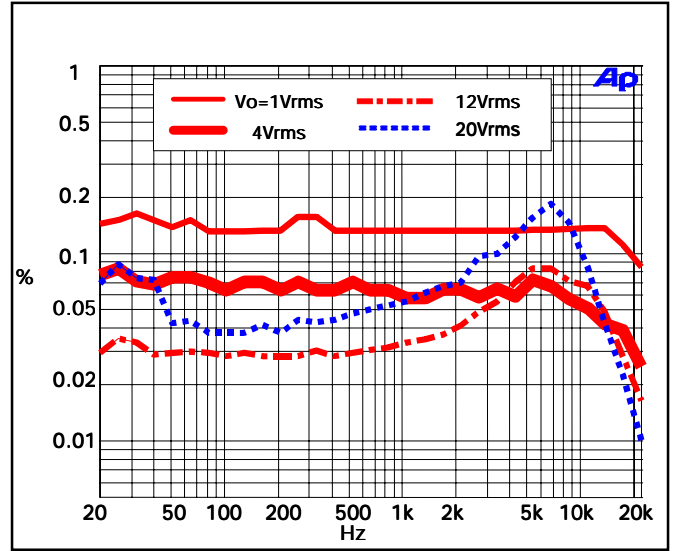


Fig. 5 THD + Noise for the amplifier with output feedback (V<sub>o</sub>: output voltage)

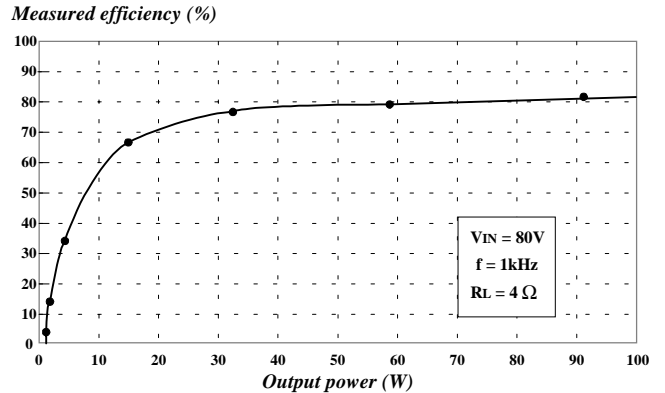


Fig. 6 Power efficiency of the implemented amplifier

## VI. CONCLUSION

This paper has introduced a novel pulse referenced error correction method, Bi-directional Saw-tooth Error Correction (BSEC) for switching audio power amplifier with digital input. The controller has several advantages:

- Wide range of error correction: Bi-directional saw-tooth makes it possible to correct amplifier duty ratio

into any value between 0 and 1. This wide error correction capability guarantees wide input operation range of audio power systems.

- No modulation index limitation: Saw-tooth width of BSEC unit is not fixed but flexible, following duty of reference pulse signal, which allows the duty to swing from 0 to 1.
- High gain of the error correction circuit: Since there is no trade-off between modulation index and BSEC unit gain, the high gain controller design is possible.
- High switching frequency: At the same operating point (same reference duty and same controller gain), the saw-tooth of BSEC controller has half the tangential slope compared with PEDEC case. This means that in the case of BSEC, the twice switching frequency is possible in view point of practical limitation of tangential slope realization.

A 100W prototype for the hardware evaluation has demonstrated that the proposed controller enables the hardware to operate with excellent THD below 0.2% for all audio frequency and power range with high efficiency.

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